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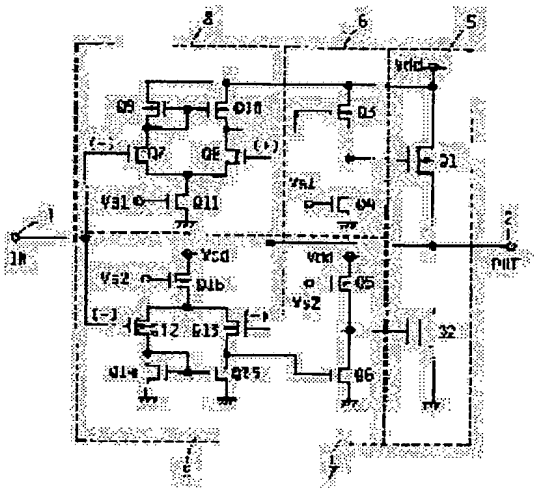
(54) MOSFET POWER AMPLIFIER

(57)Abstract:
PURPOSE: To reduce the invalid current of a power output stage, to reduce cross-over distortion and to efficiently drive a MOSFET power amplifier by providing offset stages before and behind a power output stage and providing amplifier stages amplifying input signals before and behind the offset stages.
CONSTITUTION: The positive side offset (level shift) stage 6 for PMOSFET Q1 and the negative side offset (level shift) stage 7 for NMOSFET Q2 are provided for the gate voltage bias of PMOSFET Q1 and NMOSFET Q2 in the power output stage 5. A positive side differential amplifier stage 8 is provided in the prestage of the positive side offset stage 6 and a negative side differential amplifier stage 9 in the prestage of the negative side offset stage 7. Voltage inputted to an input terminal 1 is impressed on the inverted input means of the differential amplifying stages 8 and 9. In such a case, the non- inverted input-sides of the differential amplifying stages 8 and 9 are connected to an output terminal 2, and they function as a voltage follower.



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* NOTICES *

CLAIMS

[Claim(s)]

[Claim 1] MOSFET power amplifier characterized by establishing the offset stage in the preceding paragraph of the above-mentioned power-output stage, preparing the amplification stage which amplifies an input signal in the preceding paragraph of this offset stage in the push pull type MOSFET power amplifier which the power-output stage becomes from CMOS composition, and setting up the gate bias voltage of MOSFET of the above-mentioned power-output stage in the above-mentioned offset stage.

[Claim 2] While separating and establishing the above-mentioned offset stage in the positive side offset stage for the PMOSFET sides of the above-mentioned power-output stage, and the negative side offset stage for the NMOSFET sides MOSFET power amplifier according to claim 1 characterized by having prepared the above-mentioned amplification stage as a difference input stage common to the above-mentioned positive side

offset stage and the above-mentioned negative side offset stage, or dissociating and preparing in the negative side difference input stage the positive side difference input stage for the above-mentioned positive side offset stages, and for the above-mentioned negative side offset stages.

[Claim 3] MOSFET power amplifier characterized by preparing the resister network which sets the gate bias voltage of MOSFET of the above-mentioned power-output stage as a feedback circuit in the push pull type MOSFET power amplifier which the power-output stage becomes from CMOS composition from the above-mentioned power-output stage to the amplification stage which amplifies an input signal.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] this invention relates to the MOSFET power amplifier which amplifies a sound signal in portable electrical machinery and apparatus, such as a pocket sound product, a pocket personal computer, a pocket multimedia device, and a mobile phone machine.

[0002]

[Description of the Prior Art] Although power amplification of the sound signal of a portable electrical machinery and apparatus was realized by the bipolar transistor circuit by the former, with low-battery-izing of the supply voltage to be used, the saturation voltage (Vce) between collector emitters which the bipolar transistor essentially has drops the use efficiency of output voltage, and the problem that output power becomes inadequate as a result, or a power efficiency declines is becoming large.

[0003] Then, although adding a booster circuit, carrying out the pressure

up of the supply voltage, and operating the power amplification section had been performed, the improvement of the field of a power efficiency did not progress.

[0004] On the other hand, the attempt which constitutes power amplifier using an FET element accomplished. However, in a high-fi field, although the demand of quality is applied to the field which is not severe, except when it can be made to operate on voltage high enough, it is not put in practical use.

[0005] This is because the bird clapper is unescapable to the result which consumes reactive power (based on penetration current) more than it if FET is inferior to a bipolar transistor in the capacity to drive current and it is going to drive power just like a pie Poral transistor.

[0006] By the way, the method of controlling a bias current in recent years according to an output swing is put in practical use, and the MOSFET power amplifier to which only the time of a large amplitude made current drive capacity increase, and has improved the power efficiency as shown in drawing 4 is proposed (IEEE J.SOLID STATE CIRCUITS, Vol.SC-17, no.6, pp 929-982, and Dec.1982). The circuit of this drawing 5 is called semi- source follower power amplifier, and, for one, as for an output terminal and 3, an input terminal and 2 are [the positive side amplification stage and 4] negative side amplification stages among drawing. Moreover, 5 is the power-output stage of CMOS push pull composition, and consists of PMOSFETQ1 for an output, and NMOSFETQ2 for an output.

[0007] Moreover, in such semi- source follower power amplifier, as shown in drawing 5 for the formation of power consumption reduction at the time of an input non-signal, the method of giving input offset to the amplification stages 3 and 4 is also proposed. V1 and V2 are input offset voltage (IEEEJ.SOLID STATE CIRCUITS, Vol.SC-20, no.6, pp 1200-1205,

and Dec.1982).

[0008]

[Problem(s) to be Solved by the Invention] By the way, in semi- source follower power amplifier which was described above, at the time of a non-signal, an input must be stably controlled so that the reactive current (penetration current) of the gate of MOSFETQ1 and Q2 of the power-output stage 5 decreases and a cross over distortion also decreases.

[0009] That is, if there is offset and the output voltage shifts from predetermined voltage into the amplification stage 3 and 4, the excessive reactive current flows to MOSFETQ1 and Q2 of the power-output stage 5, or a reverse bias will be carried out deeply conversely and problems, like a cross over distortion becomes large will arise.

[0010] Moreover, in the semi- source follower power amplifier shown in drawing 5 which gave offset to the input side, since the offset voltage is amplified in the amplification stages 3 and 4, although symmetric property (identity) is required of the amplification stages 3 and 4, this is difficult, and in the power-output stage 5 which consists of MOSFETQ1 and Q2, the above-mentioned reverse bias tends to become more remarkable [the distortion of a crossover] that it will be easy to become bigger.

[0011] Then, although it will be necessary to set offset voltage as a very very small value if it is going to reduce the amount of reverse biases on the contrary, it comes to be greatly influenced of the variation at the time of manufacture.

[0012] The purpose of this invention is offering the MOSFET power amplifier performs the stable offset, solves the above-mentioned problem, and realizes the few reactive current of the power-output stage, and a low cross over distortion, and it enabled it to drive efficiently.

[0013]

[Means for Solving the Problem] In the push pull type MOSFET power amplifier which the power-output stage becomes from CMOS composition, the purpose of this invention establishes the offset stage in the preceding paragraph of the above-mentioned power-output stage, prepares the amplification stage which amplifies an input signal in the preceding paragraph of this offset stage, and is attained by the MOSFET power amplifier characterized by setting up the gate bias voltage of MOSFET of the above-mentioned power-output stage in the above-mentioned offset stage.

[0014] Moreover, it comes to be attained by the MOSFET power amplifier characterized by preparing the resister network which sets the gate bias voltage of MOSFET of the above-mentioned power-output stage as a feedback circuit from the above-mentioned power-output stage to the amplification stage which amplifies an input signal in the push pull type MOSFET power amplifier which the power-output stage becomes from CMOS composition.

[0015]

[Example] Hereafter, the example of this invention is explained. Drawing 1 is the circuit diagram of the power amplifier of the 1st example. In this example, the positive side offset (level shift) stage 6 for PMOSFETQ1 and the negative side offset (level shift) stage 7 for NMOSFETQ2 are formed as an object for the gate-voltage bias of PMOSFETQ1 and NMOSFETQ2 of the power-output stage 5. And the positive side differential-amplifier stage 8 was established in the preceding paragraph of the positive side offset stage 6, the negative side differential-amplifier stage 9 was established in the preceding paragraph of the negative side offset stage 7, and the voltage inputted into the inversed input terminal of both these differential-amplifiers stages 7 and 8 at an input terminal 1 was made to impress. It connects with an output terminal 2 and the noninverting input

side of both these differential-amplifiers stages 8 and 9 functions as a BORUTE follower respectively.

[0016] The positive side offset stage 6 consists of circuits which made CMOS connection of NMOSFETQ4 of PMOSFETQ3 which undergoes the output of the positive side differential-amplifier stage 8, and constant-voltage bias, and the negative side offset stage 7 consists of circuits which made CMOS connection of NMOSFETQ6 which undergoes the output of the PMOSFETQ5 and the negative side differential-amplifier stage 9 of constant-voltage bias. Vs1 is bias voltage.

[0017] Moreover, the positive side differential-amplifier stage 8 consists of NMOSFETQ7 and Q8 by which differential connection is made, PMOSFETQ9 and Q10 by which current mirror connection is made as an active load of the differential connected circuit, and NMOSFETQ11 which functions as a source of the operating current. Vs2 is bias voltage.

[0018] Furthermore, the negative side differential-amplifier stage 9 consists of PMOSFETQ12 and Q13 by which differential connection is made, NMOSFETQ14 and Q15 by which current mirror connection is made as an active load of the differential connected circuit, and PMOSFETQ16 which functions as a source of the operating current.

[0019] Now, if voltage inputs into an input terminal 1, difference voltage with the voltage of the output terminal 2 which has returned to the noninverting input side of both the differential-amplifiers stages 8 and 9 will be amplified by the differential-amplifier stage 8 or differential amplifier 9, and MOSFETQ1 and Q2 of the power-output stage 5 will be controlled in the direction in which the voltage of an output terminal 2 becomes equal to the voltage of an input terminal 1.

[0020] Therefore, when the input of an input terminal 1 is a non-signal, the voltage of the input terminal 1 is the half (Vdd/2) of supply voltage Vdd, and the voltage appears in an output terminal 2.

[0021] At the time of this non-signal, the gate voltage of the power-output stage 5 is desirable, in order for the one smaller than the threshold (Vth) there of MOSFETQ1 and Q2 to be reactive current reduction. Both can be satisfied to set up offset the optimal although it has the relation which disagrees with decreasing a decreasing-this reactive current cross over distortion.

[0022] Then, in this example, only several V shifts the gate voltage for outputting to the power-output stage 5 in the offset stages 6 and 7 according to Vth of MOSFETQ1 and Q2 of the power-output stage 5.

[0023] for this reason -- being alike -- the offset stage 6 -- setting -- the size ratio (width-of-face W / channel length L of a channel) of MOSFETQ3 and Q4 -- moreover, in the offset stage 7, the size ratio of MOSFETQ5 and Q6 is set up suitably, and is performed

[0024] If the output voltage of the offset stage 6 will be set up at this time so that the gate voltage (Vgs) at the time of a non-signal may be set to 150mV and it will be then made a cut-off supposing the threshold (Vth) of PMOSFETQ1 of the now, for example, power output, stage 5 is 650mV, a 500mV margin can be given there.

[0025] Therefore, the input voltage range from which the drain of this PMOSFETQ1 will be in floating is 500 mV/G (however, G sum total gain of the amplification stage 6 and the differential-amplifier stage 8), and since it is made to several mV or less, it can also keep a cross over distortion small.

[0026] on the other hand, the circuit of drawing 5 mentioned above -- when dozens of mV comes out at most, the voltage which can be generated intentionally also has the minimum in the technique of giving offset voltage to the input side of the amplification stages 3 and 4 like, the voltage of this is amplified, it carries out to the gate-voltage shift of the power-output stage and it considers that the manufacture error is also

amplified, it is very difficult to control stably For example, since the input offset voltage decreases input voltage range as it is even when the gain of the amplification stages 3 and 4 is set up low and input offset voltage is made into a comparatively big value, a result which narrows the operating voltage range is brought.

[0027] Thus, in the power amplifier of the 1st example shown in this drawing 1 , it can prevent that invalid penetration current increases in the power-output stage 5. For this reason, since feedback to which the consumed electric current increases in other circuit sections at the time of about [that the idling current at the time of a non-signal can be suppressed to the small value which is the grade to which a cross over distortion does not become large], and operation is not needed, efficient offset can be performed. Moreover, since an input side is not made to generate intentional offset voltage, it can set up widely, without being influenced of offset of input voltage range, and large amplitude operation is attained.

[0028] Drawing 2 is drawing showing the power amplifier of the 2nd example. The same sign is given to the same thing as the power amplifier of the 1st example shown in drawing 1 . Here, one differential-amplifier stage 10 is used. This differential-amplifier stage 10 consists of PMOSFETQ17 and Q18 by which differential connection is made, NMOSFETQ19 and Q20 by which current mirror connection is made as an active load of the differential connected circuit, and PMOSFETQ21 which functions as a source of the operating current. Moreover, it constitutes from PMOSFETQ22 by which constant-voltage bias is carried out considering the positive side offset stage 11 as the same composition as the negative side offset stage 7, and NMOSFETQ23 which undergoes the output of the differential-amplifier stage 10.

[0029] In the power amplifier of this 2nd example, since an input side

consists of one differential-amplifier stage, compared with the case where two differential-amplifier stages explained by drawing 1 are used, the influence of the random offset error generated in about [being advantageous in cost] and two or more circuits can also be reduced.

[0030] Drawing 3 is drawing showing the power amplifier of the 3rd example. Here, in the circuit of drawing 4 mentioned above, offset is set to the feedback side of the amplification stages 3 and 4 and the power-output stage 5 by the resister network.

[0031] This offset is what consists of the resistance R1-R3 which carried out the series connection to the power supply between groundings, feedback resisters R4 and R5 connected with the common node of resistance R1 and R2, and the output terminal 2 in between, and feedback resisters R6 and R7 connected between the common node of resistance R2 and R3, and the output terminal 2. The common node of resistance R4 and R5 is connected to the noninverting input terminal of the amplification stage 3, and the common node of resistance R6 and R7 is connected to the noninverting input terminal of the amplification stage 4. Here, as resistance R1 and R3, as 10Kohm and R2, R5 can be used as 100-200ohm, and R4 and R6, and 5Kohm can be used as 100Kohm and R7.

[0032] In the 3rd example of this drawing 3 , the potential difference of [R2andVdd/(R1+R2+R3)] can be given among the ends of resistance R2. By this, the amount of relative offset of the amplification stages 3 and 4 (difference of the amount of offset) can be set up. And the amount of offset and gain of the positive side amplification stage 3 are set up by the ratio of resistance R4 and R5, and, thereby, the gate-voltage bias value of PMOSFETQ1 is determined. Moreover, the amount of offset and gain of the negative side amplification stage 4 are set up by the ratio of resistance R6 and R7, and, thereby, the gate-voltage bias value of NMOSFETQ2 is determined.

[0033] Thus, since the voltage division by the resister network is used for offset voltage generating, there is little reactive current, and it can set up now stably the offset voltage whose cross over distortion decreases flexibly to a fine comparatively small value, and can also lessen the burden given to the arrangement on a substrate etc. in that case here. In a semiconductor manufacturing process, the ejection position of this resistance can be performed at the wiring process near a final process, and the trimming which complements manufacture variations, such as a transistor, is also possible for it. Furthermore, the amount of offset can be adjusted without changing the form of a circuit, and a master slice is also possible for it.

[0034]

[Effect of the Invention] As mentioned above, according to this invention, the reactive current which has the relation of a trade-off, and offset voltage to which both of a cross over distortion are satisfied can be generated. And since the offset stage is prepared just before the power-output stage at this time, it is avoidable that the offset voltage which made it generate has a bad influence on the operating voltage range. Moreover, this offset can also be generated in the voltage division by the resister network, it can set up now flexibly stably to a fine comparatively small value, and the burden given to the arrangement on a substrate etc. in that case also decreases.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] this invention relates to the MOSFET power

amplifier which amplifies a sound signal in portable electrical machinery and apparatus, such as a pocket sound product, a pocket personal computer, a pocket multimedia device, and a mobile phone machine.

[0002]

[Description of the Prior Art] Although power amplification of the sound signal of a portable electrical machinery and apparatus was realized by the bipolar transistor circuit by the former, with low-battery-izing of the supply voltage to be used, the saturation voltage (Vce) between collector emitters which the bipolar transistor essentially has drops the use efficiency of output voltage, and the problem that output power becomes inadequate as a result, or a power efficiency declines is becoming large.

[0003] Then, although adding a booster circuit, carrying out the pressure up of the supply voltage, and operating the power amplification section had been performed, the improvement of the field of a power efficiency did not progress.

[0004] On the other hand, the attempt which constitutes power amplifier using an FET element accomplished. However, in a high-fi field, although the demand of quality is applied to the field which is not severe, except when it can be made to operate on voltage high enough, it is not put in practical use.

[0005] This is because the bird clapper is unescapable to the result which consumes reactive power (based on penetration current) more than it if FET is inferior to a bipolar transistor in the capacity to drive current and it is going to drive power just like a pie Poral transistor.

[0006] By the way, the method of controlling a bias current in recent years according to an output swing is put in practical use, and the MOSFET power amplifier to which only the time of a large amplitude made current drive capacity increase, and has improved the power efficiency as shown in drawing 4 is proposed (IEEE J.SOLID STATE CIRCUITS,

Vol.SC-17, no.6, pp 929-982, and Dec.1982). The circuit of this drawing 5 is called semi- source follower power amplifier, and, for one, as for an output terminal and 3, an input terminal and 2 are [the positive side amplification stage and 4] negative side amplification stages among drawing. Moreover, 5 is the power-output stage of CMOS push pull composition, and consists of PMOSFETQ1 for an output, and NMOSFETQ2 for an output.

[0007] Moreover, in such semi- source follower power amplifier, as shown in drawing 5 for the formation of power consumption reduction at the time of an input non-signal, the method of giving input offset to the amplification stages 3 and 4 is also proposed. V1 and V2 are input offset voltage (IEEEJ.SOLID STATE CIRCUITS, Vol.SC-20, no.6, pp 1200-1205, and Dec.1982).

[0008]

[Problem(s) to be Solved by the Invention] By the way, in semi- source follower power amplifier which was described above, at the time of a non-signal, an input must be stably controlled so that the reactive current (penetration current) of the gate of MOSFETQ1 and Q2 of the power-output stage 5 decreases and a cross over distortion also decreases.

[0009] That is, if there is offset and the output voltage shifts from predetermined voltage into the amplification stage 3 and 4, the excessive reactive current flows to MOSFETQ1 and Q2 of the power-output stage 5, or a reverse bias will be carried out deeply conversely and problems, like a cross over distortion becomes large will arise.

[0010] Moreover, in the semi- source follower power amplifier shown in drawing 5 which gave offset to the input side, since the offset voltage is amplified in the amplification stages 3 and 4, although symmetric property (identity) is required of the amplification stages 3 and 4, this is difficult,

and in the power-output stage 5 which consists of MOSFETQ1 and Q2, the above-mentioned reverse bias tends to become more remarkable [the distortion of a crossover] that it will be easy to become bigger.

[0011] Then, although it will be necessary to set offset voltage as a very very small value if it is going to reduce the amount of reverse biases on the contrary, it comes to be greatly influenced of the variation at the time of manufacture.

[0012] The purpose of this invention is offering the MOSFET power amplifier performs the stable offset, solves the above-mentioned problem, and realizes the few reactive current of the power-output stage, and a low cross over distortion, and it enabled it to drive efficiently.

[0013]

[Means for Solving the Problem] In the push pull type MOSFET power amplifier which the power-output stage becomes from CMOS composition, the purpose of this invention establishes the offset stage in the preceding paragraph of the above-mentioned power-output stage, prepares the amplification stage which amplifies an input signal in the preceding paragraph of this offset stage, and is attained by the MOSFET power amplifier characterized by setting up the gate bias voltage of MOSFET of the above-mentioned power-output stage in the above-mentioned offset stage.

[0014] Moreover, it comes to be attained by the MOSFET power amplifier characterized by preparing the resister network which sets the gate bias voltage of MOSFET of the above-mentioned power-output stage as a feedback circuit from the above-mentioned power-output stage to the amplification stage which amplifies an input signal in the push pull type MOSFET power amplifier which the power-output stage becomes from CMOS composition.

[0015]

[Example] Hereafter, the example of this invention is explained. Drawing 1 is the circuit diagram of the power amplifier of the 1st example. In this example, the positive side offset (level shift) stage 6 for PMOSFETQ1 and the negative side offset (level shift) stage 7 for NMOSFETQ2 are formed as an object for the gate-voltage bias of PMOSFETQ1 and NMOSFETQ2 of the power-output stage 5. And the positive side differential-amplifier stage 8 was established in the preceding paragraph of the positive side offset stage 6, the negative side differential-amplifier stage 9 was established in the preceding paragraph of the negative side offset stage 7, and the voltage inputted into the inversed input terminal of both these differential-amplifiers stages 7 and 8 at an input terminal 1 was made to impress. It connects with an output terminal 2 and the noninverting input side of both these differential-amplifiers stages 8 and 9 functions as a BORUTE follower respectively.

[0016] The positive side offset stage 6 consists of circuits which made CMOS connection of NMOSFETQ4 of PMOSFETQ3 which undergoes the output of the positive side differential-amplifier stage 8, and constant-voltage bias, and the negative side offset stage 7 consists of circuits which made CMOS connection of NMOSFETQ6 which undergoes the output of the PMOSFETQ5 and the negative side differential-amplifier stage 9 of constant-voltage bias. Vs1 is bias voltage.

[0017] Moreover, the positive side differential-amplifier stage 8 consists of NMOSFETQ7 and Q8 by which differential connection is made, PMOSFETQ9 and Q10 by which current mirror connection is made as an active load of the differential connected circuit, and NMOSFETQ11 which functions as a source of the operating current. Vs2 is bias voltage.

[0018] Furthermore, the negative side differential-amplifier stage 9 consists of PMOSFETQ12 and Q13 by which differential connection is made, NMOSFETQ14 and Q15 by which current mirror connection is made

as an active load of the differential connected circuit, and PMOSFETQ16 which functions as a source of the operating current.

[0019] Now, if voltage inputs into an input terminal 1, difference voltage with the voltage of the output terminal 2 which has returned to the noninverting input side of both the differential-amplifiers stages 8 and 9 will be amplified by the differential-amplifier stage 8 or differential amplifier 9, and MOSFETQ1 and Q2 of the power-output stage 5 will be controlled in the direction in which the voltage of an output terminal 2 becomes equal to the voltage of an input terminal 1.

[0020] Therefore, when the input of an input terminal 1 is a non-signal, the voltage of the input terminal 1 is the half (Vdd/2) of supply voltage Vdd, and the voltage appears in an output terminal 2.

[0021] At the time of this non-signal, the gate voltage of the power-output stage 5 is desirable, in order for the one smaller than the threshold (Vth) there of MOSFETQ1 and Q2 to be reactive current reduction. Both can be satisfied to set up offset the optimal although it has the relation which disagrees with decreasing a decreasing-this reactive current cross over distortion.

[0022] Then, in this example, only several V shifts the gate voltage for outputting to the power-output stage 5 in the offset stages 6 and 7 according to Vth of MOSFETQ1 and Q2 of the power-output stage 5.

[0023] for this reason -- being alike -- the offset stage 6 -- setting -- the size ratio (width-of-face W / channel length L of a channel) of MOSFETQ3 and Q4 -- moreover, in the offset stage 7, the size ratio of MOSFETQ5 and Q6 is set up suitably, and is performed

[0024] If the output voltage of the offset stage 6 will be set up at this time so that the gate voltage (Vgs) at the time of a non-signal may be set to 150mV and it will be then made a cut-off supposing the threshold (Vth) of PMOSFETQ1 of the now, for example, power output, stage 5 is 650mV, a

500mV margin can be given there.

[0025] Therefore, the input voltage range from which the drain of this PMOSFETQ1 will be in floating is 500 mV/G (however, G sum total gain of the amplification stage 6 and the differential-amplifier stage 8), and since it is made to several mV or less, it can also keep a cross over distortion small.

[0026] on the other hand, the circuit of drawing 5 mentioned above -- when dozens of mV comes out at most, the voltage which can be generated intentionally also has the minimum in the technique of giving offset voltage to the input side of the amplification stages 3 and 4 like, the voltage of this is amplified, it carries out to the gate-voltage shift of the power-output stage and it considers that the manufacture error is also amplified, it is very difficult to control stably For example, since the input offset voltage decreases input voltage range as it is even when the gain of the amplification stages 3 and 4 is set up low and input offset voltage is made into a comparatively big value, a result which narrows the operating voltage range is brought.

[0027] Thus, in the power amplifier of the 1st example shown in this drawing 1 , it can prevent that invalid penetration current increases in the power-output stage 5. For this reason, since feedback to which the consumed electric current increases in other circuit sections at the time of about [that the idling current at the time of a non-signal can be suppressed to the small value which is the grade to which a cross over distortion does not become large], and operation is not needed, efficient offset can be performed. Moreover, since an input side is not made to generate intentional offset voltage, it can set up widely, without being influenced of offset of input voltage range, and large amplitude operation is attained.

[0028] Drawing 2 is drawing showing the power amplifier of the 2nd

example. The same sign is given to the same thing as the power amplifier of the 1st example shown in drawing 1 . Here, one differential-amplifier stage 10 is used. This differential-amplifier stage 10 consists of PMOSFETQ17 and Q18 by which differential connection is made, NMOSFETQ19 and Q20 by which current mirror connection is made as an active load of the differential connected circuit, and PMOSFETQ21 which functions as a source of the operating current. Moreover, it constitutes from PMOSFETQ22 by which constant-voltage bias is carried out considering the positive side offset stage 11 as the same composition as the negative side offset stage 7, and NMOSFETQ23 which undergoes the output of the differential-amplifier stage 10.

[0029] In the power amplifier of this 2nd example, since an input side consists of one differential-amplifier stage, compared with the case where two differential-amplifier stages explained by drawing 1 are used, the influence of the random offset error generated in about [being advantageous in cost] and two or more circuits can also be reduced.

[0030] Drawing 3 is drawing showing the power amplifier of the 3rd example. Here, in the circuit of drawing 4 mentioned above, offset is set to the feedback side of the amplification stages 3 and 4 and the power-output stage 5 by the resister network.

[0031] This offset is what consists of the resistance R1-R3 which carried out the series connection to the power supply between groundings, feedback resisters R4 and R5 connected with the common node of resistance R1 and R2, and the output terminal 2 in between, and feedback resisters R6 and R7 connected between the common node of resistance R2 and R3, and the output terminal 2. The common node of resistance R4 and R5 is connected to the noninverting input terminal of the amplification stage 3, and the common node of resistance R6 and R7 is connected to the noninverting input terminal of the amplification stage 4. Here, as

resistance R1 and R3, as 10Kohm and R2, R5 can be used as 100-200ohm, and R4 and R6, and 5Kohm can be used as 100Kohm and R7.

[0032] In the 3rd example of this drawing 3 , the potential difference of [R2andVdd/(R1+R2+R3)] can be given among the ends of resistance R2. By this, the amount of relative offset of the amplification stages 3 and 4 (difference of the amount of offset) can be set up. And the amount of offset and gain of the positive side amplification stage 3 are set up by the ratio of resistance R4 and R5, and, thereby, the gate-voltage bias value of PMOSFETQ1 is determined. Moreover, the amount of offset and gain of the negative side amplification stage 4 are set up by the ratio of resistance R6 and R7, and, thereby, the gate-voltage bias value of NMOSFETQ2 is determined.

[0033] Thus, since the voltage division by the resister network is used for offset voltage generating, there is little reactive current, and it can set up now stably the offset voltage whose cross over distortion decreases flexibly to a fine comparatively small value, and can also lessen the burden given to the arrangement on a substrate etc. in that case here. In a semiconductor manufacturing process, the ejection position of this resistance can be performed at the wiring process near a final process, and the trimming which complements manufacture variations, such as a transistor, is also possible for it. Furthermore, the amount of offset can be adjusted without changing the form of a circuit, and a master slice is also possible for it.

[0034]

[Effect of the Invention] As mentioned above, according to this invention, the reactive current which has the relation of a trade-off, and offset voltage to which both of a cross over distortion are satisfied can be generated. And since the offset stage is prepared just before the power-output stage at this time, it is avoidable that the offset voltage

which made it generate has a bad influence on the operating voltage range. Moreover, this offset can also be generated in the voltage division by the resister network, it can set up now flexibly stably to a fine comparatively small value, and the burden given to the arrangement on a substrate etc. in that case also decreases.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the circuit diagram of the power amplifier of the 1st example of this invention.

[Drawing 2] It is the circuit diagram of the power amplifier of the 2nd example of this invention.

[Drawing 3] It is the circuit diagram of the power amplifier of the 3rd example of this invention.

[Drawing 4] It is the block diagram of the conventional power amplifier.

[Drawing 5] It is the block diagram of another conventional power amplifier.

[Description of Notations]

1: An input terminal, 2:output terminal, the 3:positive side amplification stage, 4:negative side amplification stage, 5:power-output stage, the 6:positive side offset stage, 7:negative side offset stage, the 8:positive side difference input stage, 9 : negative side difference input stage, 10:1 difference input stages.

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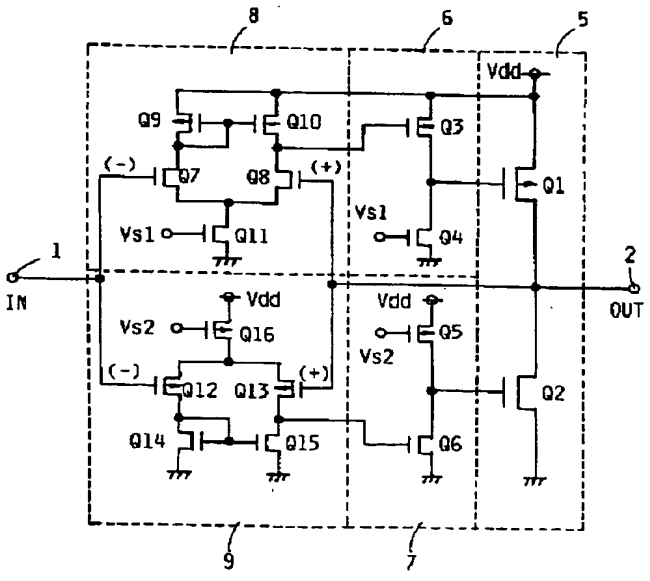
(54)【発明の名称】ＭＯＳＦＥＴ電力増幅器

(57)【要約】

【目的】　無効貫通電流の減少とクロスオーバ歪の減少を達成できるオフセットを行なった電力増幅器を提供すること。

【構成】　電力出力段５がＣＭＯＳ構成でなるプッシュプル型のＭＯＳＦＥＴ電力増幅器において、電力出力段５の直前にオフセット段６、７を設け、その電力出力段５のＭＯＳＦＥＴのゲート電圧バイアスを行なう。



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【特許請求の範囲】

【請求項１】　電力出力段がＣＭＯＳ構成からなるプッシュプル型のＭＯＳＦＥＴ電力増幅器において、上記電力出力段の前段にオフセット段を設け、該オフセット段の前段に入力信号を増幅する増幅段を設け、上記オフセット段において上記電力出力段のＭＯＳＦＥＴのゲートバイアス電圧を設定するようにしたことを特徴とするＭＯＳＦＥＴ電力増幅器。

【請求項２】　上記オフセット段を上記電力出力段のＰＭＯＳＦＥＴ側用の正側オフセット段と、ＮＭＯＳＦＥＴ側用の負側オフセット段に分離して設けると共に、上記増幅段を上記正側オフセット段と上記負側オフセット段に共通の差動入力段として設け、又は上記正側オフセット段用の正側差動入力段と上記負側オフセット段用の負側差動入力段に分離して設けたことを特徴とする請求項１に記載のＭＯＳＦＥＴ電力増幅器。

【請求項３】　電力出力段がＣＭＯＳ構成からなるプッシュプル型のＭＯＳＦＥＴ電力増幅器において、入力信号を増幅する増幅段への上記電力出力段からの帰還回路に、上記電力出力段のＭＯＳＦＥＴのゲートバイアス電圧を設定する抵抗ネットワークを設けたことを特徴とするＭＯＳＦＥＴ電力増幅器。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、携帯音響製品、携帯パーソナルコンピュータ、携帯マルチメディア機器、移動電話機等の携帯用電気機器において、音声信号を増幅するＭＯＳＦＥＴ電力増幅器に関するものである。

【０００２】

【従来の技術】携帯用電気機器の音声信号の電力増幅は、従来ではバイポーラトランジスタ回路によって実現されていたが、使用する電源電圧の低電圧化に伴って、バイポーラトランジスタが本質的に持っているコレクタ・エミッタ間飽和電圧（Ｖｃｅ）が出力電圧の利用効率を落してしまい、結果として出力パワーが不十分となったり、電力効率が低下するという問題が大きくなってきた。

【０００３】そこで、昇圧回路を付加し、電源電圧を昇圧して電力増幅部を動作させることが行なわれてきたが、電力効率の面の改善は進まなかった。

【０００４】一方、ＦＥＴ素子を使用して電力増幅器を構成する試みが成された。しかし、品質の要求が厳しくない分野には応用されているものの、ハイファイ分野では充分に高い電圧で動作させることができる場合以外は、実用化されていない。

【０００５】これは、ＦＥＴは電流を駆動する能力がバイポーラトランジスタに劣っており、バイポーラトランジスタ並に電力を駆動しようとすると、それ以上に無効電力（貫通電流による）を消費する結果になることが不可避であるからである。

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【０００６】ところで、近年バイアス電流を出力振幅に応じて制御する方法を実用化して、大振幅のときだけ電流駆動能力を増加させて電力効率を改善した、図４に示すようなＭＯＳＦＥＴ電力増幅器が提案されている（IEEE J.SOLID STATE CIRCUITS,Vol.SC-17,no.6,pp929-982, Dec.1982 ）。この図５の回路は準ソースホロワ電力増幅器とよばれるもので、図中、１は入力端子、２は出力端子、３は正側増幅段、４は負側増幅段である。また５はＣＭＯＳプッシュプル構成の電力出力段であって、出力用ＰＭＯＳＦＥＴＱ１と出力用ＮＭＯＳＦＥＴＱ２とからなる。

【０００７】またこのような準ソースホロワ電力増幅器においては、入力無信号時の消費電力低減化のために、図５に示すように、増幅段３、４に対して入力オフセットを持たせる方法も提案されている。Ｖ１、Ｖ２が入力オフセット電圧である（IEEEJ.SOLID STATE CIRCUITS,Vol.SC-20,no.6,pp1200-1205, Dec.1982 ）。

【０００８】

【発明が解決しようとする課題】ところで、上記したような準ソースホロワ電力増幅器においては、入力が無信号時には電力出力段５のＭＯＳＦＥＴＱ１、Ｑ２のゲートは、無効電流（貫通電流）が少なくなり、且つクロスオーバ歪も少なくなるように、安定的に制御されなければならない。

【０００９】すなわち、増幅段３、４内にオフセットがあってその出力電圧が所定の電圧からシフトしてしまうと、電力出力段５のＭＯＳＦＥＴＱ１、Ｑ２に過大な無効電流が流れたり、逆に深く逆バイアスされてクロスオーバー歪が大きくなる等の問題が起こる。

【００１０】また、入力側にオフセットを持たせた図５に示す準ソースホロワ電力増幅器では、そのオフセット電圧が増幅段３、４で増幅されるため、増幅段３、４に対称性（同一性）が要求されるがこれは困難であり、ＭＯＳＦＥＴＱ１、Ｑ２からなる電力出力段５では上記した逆バイアスはより大きなものとなり易くクロスオーバの歪はより顕著となり易い。

【００１１】そこで、反対に逆バイアス量を低減しようとするとオフセット電圧をごく微少な値に設定する必要が生じるが、製造時のバラツキの影響を大きく受けるようになる。

【００１２】本発明の目的は、安定したオフセットを行なって、上記した問題を解決し、電力出力段の少無効電流、低クロスオーバ歪を実現し、効率的に駆動できるようにしたＭＯＳＦＥＴ電力増幅器を提供することである。

【００１３】

【課題を解決するための手段】本発明の目的は、電力出力段がＣＭＯＳ構成からなるプッシュプル型のＭＯＳＦＥＴ電力増幅器において、上記電力出力段の前段にオフセット段を設け、該オフセット段の前段に入力信号を増

幅する増幅段を設け、上記オフセット段において上記電力出力段のＭＯＳＦＥＴのゲートバイアス電圧を設定するようにしたことを特徴とするＭＯＳＦＥＴ電力増幅器によって達成される。

【００１４】また、電力出力段がＣＭＯＳ構成からなるプッシュプル型のＭＯＳＦＥＴ電力増幅器において、入力信号を増幅する増幅段への上記電力出力段からの帰還回路に、上記電力出力段のＭＯＳＦＥＴのゲートバイアス電圧を設定する抵抗ネットワークを設けたことを特徴とするＭＯＳＦＥＴ電力増幅器によっても達成されるようになる。

【００１５】

【実施例】以下、本発明の実施例について説明する。図１はその第１の実施例の電力増幅器の回路図である。本実施例では、電力出力段５のＰＭＯＳＦＥＴＱ１とＮＭＯＳＦＥＴＱ２のゲート電圧バイアス用として、ＰＭＯＳＦＥＴＱ１用の正側オフセット（レベルシフト）段６、ＮＭＯＳＦＥＴＱ２用の負側オフセット（レベルシフト）段７を設けている。そして、その正側オフセット段６の前段に正側差動増幅段８を、負側オフセット段７の前段に負側差動増幅段９を設け、この両差動増幅段７、８の反転入力端子に入力端子１に入力する電圧を印加させた。この両差動増幅段８、９の非反転入力側は出力端子２に接続され、各々ボルテーホロワとして機能する。

【００１６】正側オフセット段６は正側差動増幅段８の出力を受けるＰＭＯＳＦＥＴＱ３と定電圧バイアスのＮＭＯＳＦＥＴＱ４をＣＭＯＳ接続した回路から構成され、負側オフセット段７は定電圧バイアスのＰＭＯＳＦＥＴＱ５と負側差動増幅段９の出力を受けるＮＭＯＳＦＥＴＱ６をＣＭＯＳ接続した回路から構成される。Ｖｓ１はバイアス電圧である。

【００１７】また、正側差動増幅段８は、差動接続されるＮＭＯＳＦＥＴＱ７、Ｑ８、その差動接続回路の能動負荷としてカレントミラー接続されるＰＭＯＳＦＥＴＱ９、Ｑ１０、動作電流源として機能するＮＭＯＳＦＥＴＱ１１から構成される。Ｖｓ２はバイアス電圧である。

【００１８】更に、負側差動増幅段９は、差動接続されるＰＭＯＳＦＥＴＱ１２、Ｑ１３、その差動接続回路の能動負荷としてカレントミラー接続されるＮＭＯＳＦＥＴＱ１４、Ｑ１５、動作電流源として機能するＰＭＯＳＦＥＴＱ１６から構成されている。

【００１９】さて、入力端子１に電圧が入力すると、両差動増幅段８、９の非反転入力側に帰還されている出力端子２の電圧との差電圧がその差動増幅段８又は差動増幅器９で増幅され、出力端子２の電圧が入力端子１の電圧に等しくなる方向に電力出力段５のＭＯＳＦＥＴＱ１、Ｑ２が制御される。

【００２０】よって、入力端子１の入力が無信号のときは、その入力端子１の電圧は電源電圧Ｖｄｄの半分（Ｖｄｄ／２）であり、その電圧が出力端子２に現れる。

【００２１】この無信号時には、電力出力段５のゲート電圧は、そこのＭＯＳＦＥＴＱ１、Ｑ２の閾値（Ｖｔｈ）よりも小さい方が無効電流低減のためには望ましい。この無効電流を減少させることクロスオーバ歪を減少させることとは相反する関係にあるが、オフセットを最適に設定することで両者を満足させることができる。

【００２２】そこでこの実施例では、オフセット段６、７において電力出力段５に出力するためのゲート電圧をその電力出力段５のＭＯＳＦＥＴＱ１、Ｑ２のＶｔｈに応じて数Ｖだけシフトさせてやる。

【００２３】このためには、オフセット段６においては、ＭＯＳＦＥＴＱ３とＱ４のサイズ比（チャンネルの幅Ｗ／チャンネル長Ｌ）を、またオフセット段７においてはＭＯＳＦＥＴＱ５とＱ６のサイズ比を適宜設定して行なう。

【００２４】いま、例えば、電力出力段５のＰＭＯＳＦＥＴＱ１の閾値（Ｖｔｈ）が６５０ｍＶであるとすると、このときは、無信号時のゲート電圧（Ｖｇｓ）が１５０ｍＶになるようにオフセット段６の出力電圧を設定して、そのときカットオフにさせれば、５００ｍＶの余裕をそこに持たせることができる。

【００２５】よって、このＰＭＯＳＦＥＴＱ１のドレインがフローティング状態になる入力電圧範囲は、５００ｍＶ／Ｇ（但しＧは増幅段６と差動増幅段８の合計ゲイン）であり、数ｍＶ以下にできることから、クロスオーバ歪も小さく保つことができる。

【００２６】これに対して、前述した図５の回路ように増幅段３、４の入力側にオフセット電圧を与える手法においては、意図的に発生できる電圧は最小でも数十ｍＶがせいぜいであり、これを電圧増幅して電力出力段のゲート電圧シフト用とした場合、製造誤差も増幅されていることを考えると、安定的に制御するのは極めて難しい。例えば、増幅段３、４のゲインを低く設定して入力オフセット電圧を比較的大きな値にした場合でも、その入力オフセット電圧がそのまま入力電圧範囲を減少させるので、動作電圧範囲を狭める結果となる。

【００２７】このように、この図１に示す第１の実施例の電力増幅器では、電力出力段５に無効な貫通電流が増大することを防止することができる。このため、無信号時のアイドリング電流をクロスオーバ歪が大きくならない程度の小さな値に抑えることができるばかりか、動作時においても他の回路部で消費電流が増大するような帰還を必要としないので、効率的なオフセットができる。また、入力側に意図的なオフセット電圧を発生させるものではないので、入力電圧範囲をオフセットの影響を受けずに広く設定でき、大振幅動作が可能となる。

【００２８】図２は第２の実施例の電力増幅器を示す図である。図１に示した第１の実施例の電力増幅器と同一のものには同一の符号を付している。ここでは、１系統

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の差動増幅段１０を使用している。この差動増幅段１０は、差動接続されるＰＭＯＳＦＥＴＱ１７、Ｑ１８、その差動接続回路の能動負荷としてカレントミラー接続されるＮＭＯＳＦＥＴＱ１９、Ｑ２０、動作電流源として機能するＰＭＯＳＦＥＴＱ２１から構成されている。また、正側オフセット段１１を負側オフセット段７と同様な構成として、定電圧バイアスされるＰＭＯＳＦＥＴＱ２２、差動増幅段１０の出力を受けるＮＭＯＳＦＥＴＱ２３から構成している。

【００２９】この第２の実施例の電力増幅器では、入力側が１系統の差動増幅段で構成されるので、図１で説明した２系統の差動増幅段を使用する場合に比べて、コスト的に有利であるばかりか、２系統以上の回路に発生するランダムなオフセット誤差の影響を低減することもできる。

【００３０】図３は第３の実施例の電力増幅器を示す図である。ここでは、前述した図４の回路において、増幅段３、４と電力出力段５の帰還側に抵抗ネットワークによりオフセットを設定している。

【００３１】このオフセットは、電源と接地間に直列接続した抵抗Ｒ１～Ｒ３、抵抗Ｒ１とＲ２の共通接続点と出力端子２と間に接続した帰還抵抗Ｒ４、Ｒ５、抵抗Ｒ２とＲ３の共通接続点と出力端子２との間に接続した帰還抵抗Ｒ６、Ｒ７からなるものであり、抵抗Ｒ４とＲ５の共通接続点を増幅段３の非反転入力端子に、抵抗Ｒ６とＲ７の共通接続点を増幅段４の非反転入力端子に接続している。ここで、抵抗Ｒ１、Ｒ３としては例えば１０ＫΩ、Ｒ２として１００～２００Ω、Ｒ４、Ｒ６として１００ＫΩ、Ｒ５、Ｒ７として５ＫΩが使用できる。

【００３２】この図３の第３の実施例では、抵抗Ｒ２の両端間に、［Ｒ２・Ｖｄｄ／（Ｒ１＋Ｒ２＋Ｒ３）］の電位差を持たせることができる。これによって、増幅段３と４の相対的オフセット量（オフセット量の差）を設定することができる。そして、正側増幅段３のオフセット量やゲインは抵抗Ｒ４、Ｒ５の比により設定され、これによりＰＭＯＳＦＥＴＱ１のゲート電圧バイアス値が決定される。また、負側増幅段４のオフセット量やゲインは抵抗Ｒ６、Ｒ７の比により設定され、これによりＮＭＯＳＦＥＴＱ２のゲート電圧バイアス値が決定される。

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【００３３】このように、ここではオフセット電圧発生のために抵抗ネットワークによる電圧分割を利用しているので、無効電流が少なく、且つクロスオーバ歪の少なくなるオフセット電圧をきめ細かに比較的小さい値まで安定的に柔軟に設定できるようになり、その際に基板上の配置等に与える負担も少なくできる。この抵抗の取り出し位置は半導体製造工程において、最終工程に近い配線工程で行なうことができ、トランジスタ等の製造バラツキを補完するトリミングも可能である。更に、オフセット量は回路の形を替えずに調整可能であり、マスタスライスも可能である。

【００３４】

【発明の効果】以上から本発明によれば、トレードオフの関係にある無効電流とクロスオーバ歪の両者を満足させるようなオフセット電圧を発生させることができる。そしてこのとき、オフセット段を電力出力段の直前に設けるので、発生させたオフセット電圧が動作電圧範囲に悪影響を及ぼすことを回避できる。またこのオフセットを抵抗ネットワークによる電圧分割で発生させることもでき、きめ細かに比較的小さい値まで安定的に柔軟に設定できるようになり、その際に基板上の配置等に与える負担も少なくなる。

【図面の簡単な説明】

【図１】　本発明の第１の実施例の電力増幅器の回路図である。

【図２】　本発明の第２の実施例の電力増幅器の回路図である。

【図３】　本発明の第３の実施例の電力増幅器の回路図である。

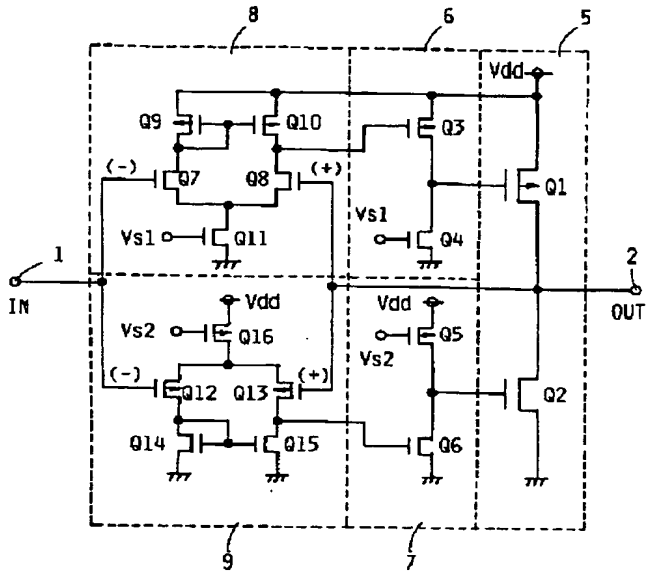
【図４】　従来の電力増幅器のブロック図である。

【図５】　従来の別の電力増幅器のブロック図である。

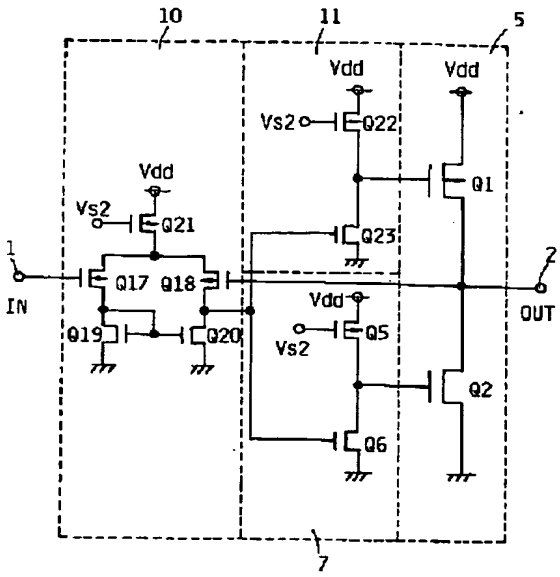
【符号の説明】

１：入力端子、２：出力端子、３：正側増幅段、４：負側増幅段、５：電力出力段、６：正側オフセット段、７：負側オフセット段、８：正側差動入力段、９：負側差動入力段、１０：１系統の差動入力段。

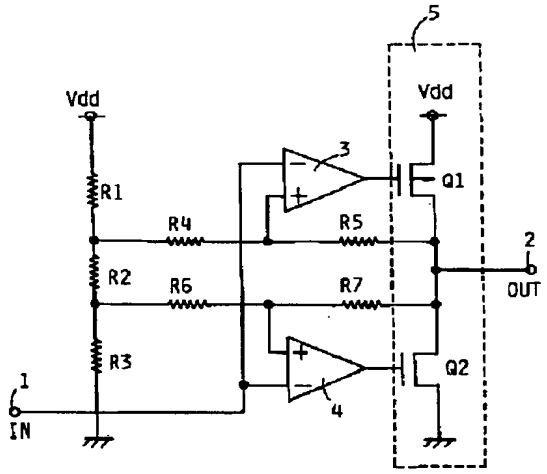
【図１】


8
6
5
Vdd
Q9
Q10
Q3
(-)
Q7
Q8
(+)
Q1
Vs1
Q11
Vs1
Q4
1
IN
2
OUT
Vdd
Vdd
Vs2
Q16
Q5
Vs2
(-)
Q12
Q13
(+)
Q2
Q14
Q15
Q6
9
7

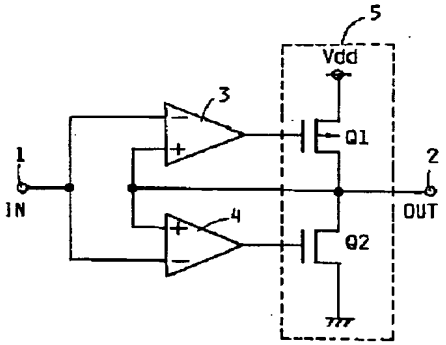
【図２】


10
11
5
Vdd
Vdd
Vs2
Q22
Q1
Vdd
Vs2
Q21
Q23
1
Q17
Q18
2
IN
OUT
Vdd
Q19
Q20
Vs2
Q5
Q2
Q6
7

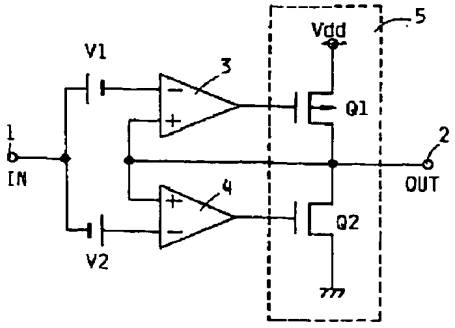
【図３】


5
Vdd
Vdd
3
R1
Q1
R4
R5
2
R2
R6
R7
OUT
R3
Q2
1
4
IN

【図４】


5
Vdd
3
Q1
1
2
IN
OUT
4
Q2

【図５】


Vdd
5
V1
3
Q1
1
2
IN
OUT
4
Q2
V2

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